PSMNR90-40YSN

N-channel 40 V, 1 mOhm, standard level MOSFET in LFPAK56

25 August 2023 **Preliminary data sheet**

1. General description

320 Amp, standard level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 320 A continuous $I_{D(max)}$
- Avalanche rated, 100% tested
- Low-spiking, allowing for high system efficiency and low EMI designs
- Optimised body-diode, gives low V_{SD} and soft switching without the associated high I_{DSS} leakage
- High reliability LFPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints for ultimate reliability
- Low parasitic inductance and resistance

3. Applications

- High-performance synchronous rectification
- DC-to-DC converters
- High performance and high efficiency server power supply
- Brushless DC motor control
- Battery protection
- Load-switch
- eFuse

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	320	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	268	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 13		[tbd]	0.81	0.97	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 14		[tbd]	1.25	1.57	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 15; Fig. 16		[tbd]	55	[tbd]	nC
$Q_{G(tot)}$	total gate charge			[tbd]	159	[tbd]	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 67.5 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 252 µs; Fig. 4	[2]	-	-	443	mJ
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 19	[3]	-	23.5	-	nC

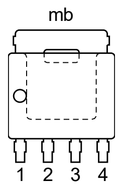
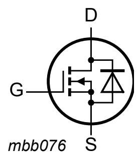
[1] 320 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and op

[2] Protected by 100% test.

[3] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR90-40YSN	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR90-40YSN	N9040S

8. Limiting values

Table 5. Limiting values

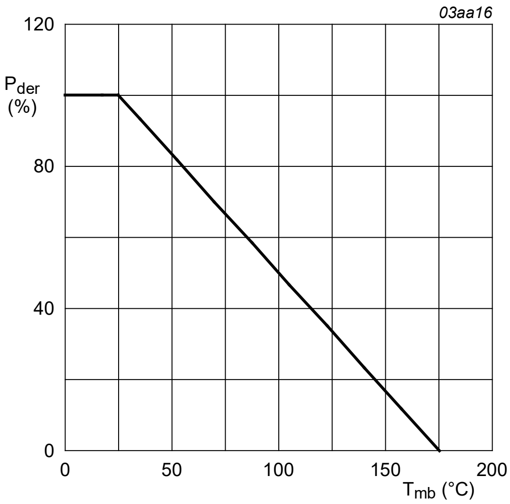
In accordance with the Absolute Maximum Rating System (IEC 60134).T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C	-	40	V

Symbol	Parameter	Conditions		Min	Max	Unit
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	268	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	320	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	262	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	1483	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[2]	-	190	A
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	268	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1483	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 67.5 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 252 µs; Fig. 4	[2]	-	443	mJ

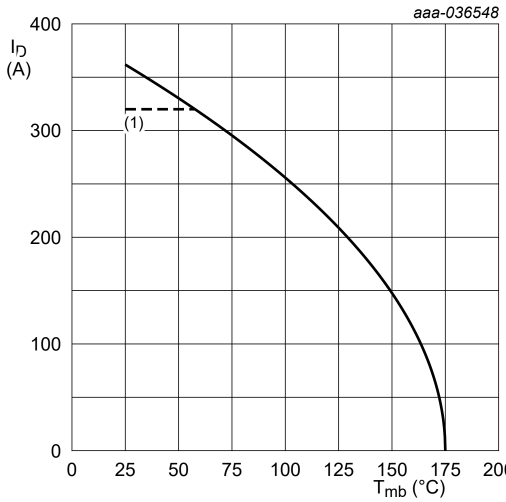
[1] 320 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and op

[2] Protected by 100% test.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

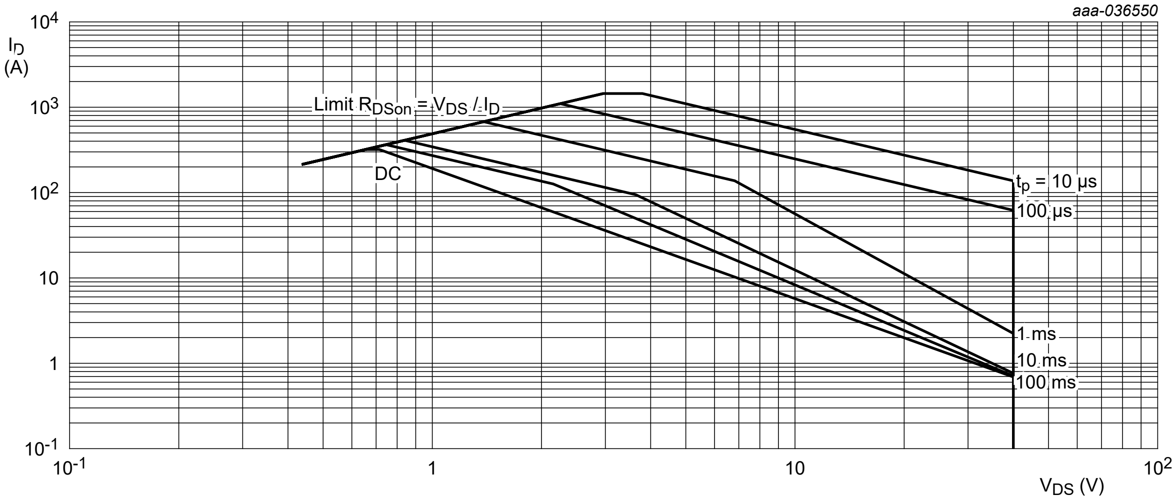
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V_{GS} ≥ 10 V

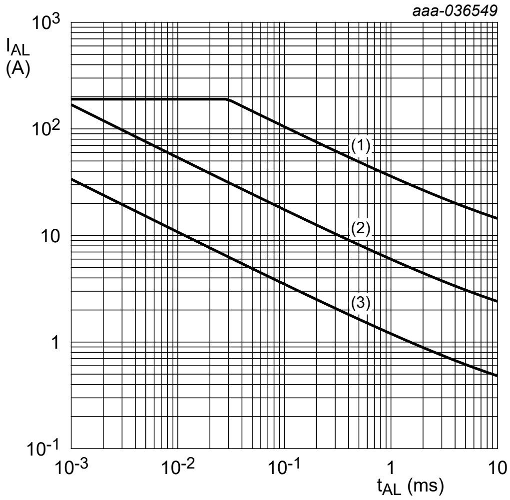
(1) 320 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.48	0.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6		-	50	-	K/W
		Fig. 7		-	125	-	K/W

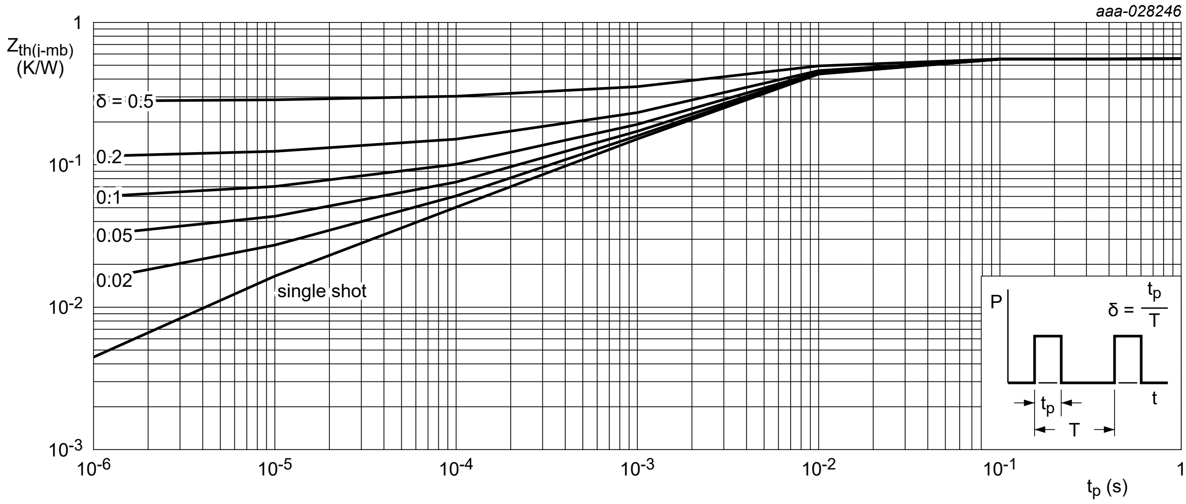


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

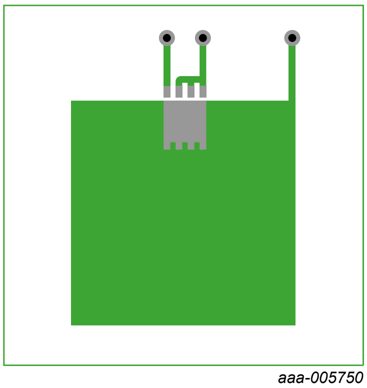


Fig. 6. PCB layout for thermal resistance junction to ambient 1” square pad; FR4 Board; 2oz copper

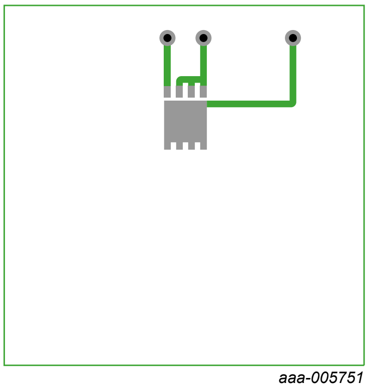


Fig. 7. PCB layout for thermal resistance junction to ambient minimum footprint;FR4 board; 2oz copper

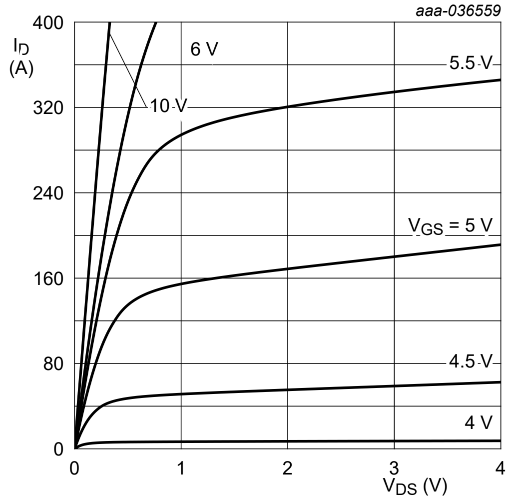
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	43	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		-	40	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 11; Fig. 12		2.4	3	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 12		-	-	4.3	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 12		1	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.1	1	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	1.06	10	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA

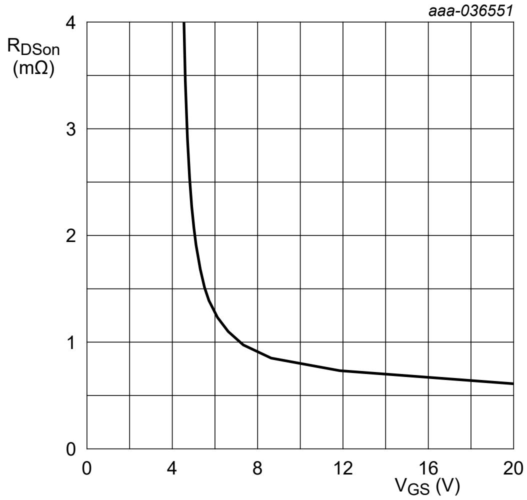
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 13		[tbd]	0.81	0.97	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 14		[tbd]	1.15	1.44	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 14		[tbd]	1.25	1.57	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 14		[tbd]	1.52	1.95	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.2	0.63	1.6	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 15; Fig. 16		[tbd]	159	[tbd]	nC
Q_{GS}	gate-source charge			[tbd]	30	[tbd]	nC
Q_{GD}	gate-drain charge			[tbd]	55	[tbd]	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 17		-	8196	[tbd]	pF
C_{oss}	output capacitance			-	1727	[tbd]	pF
C_{rss}	reverse transfer capacitance			-	736	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	25	-	ns
t_r	rise time			-	50	-	ns
$t_{d(off)}$	turn-off delay time			-	79	-	ns
t_f	fall time			-	49	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 18		-	0.79	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 19		-	34	-	ns
Q_r	recovered charge		[1]	-	23.5	-	nC

[1] includes capacitive recovery



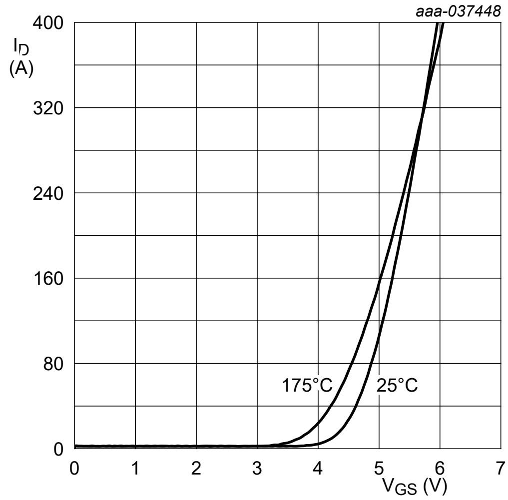
T_j = 25 °C

Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values



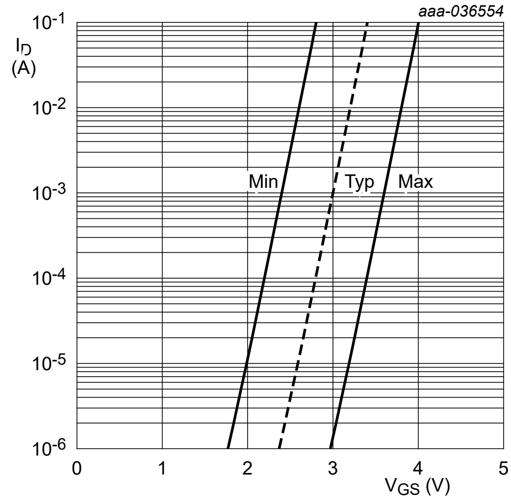
T_j = 25 °C; I_D = 25 A

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



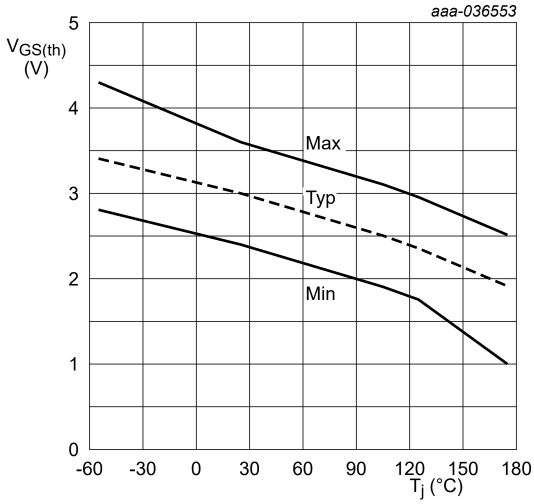
V_{DS} = 8 V

Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values



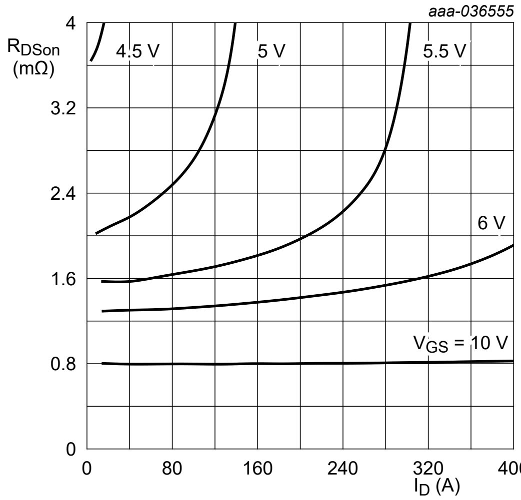
T_j = 25 °C; V_{DS} = 5 V

Fig. 11. Sub-threshold drain current as a function of gate-source voltage



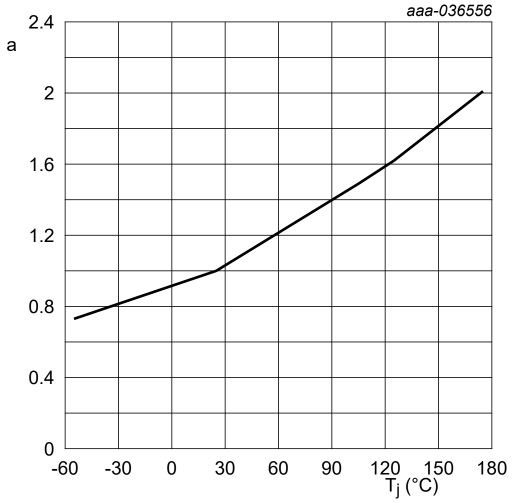
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 12. Gate-source threshold voltage as a function of junction temperature



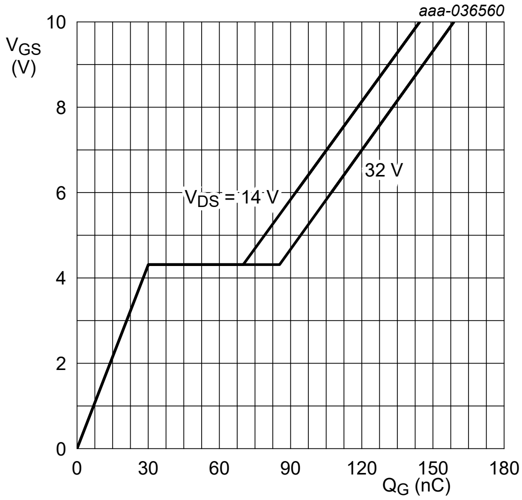
T_j = 25 °C

Fig. 13. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 14. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 15. Gate-source voltage as a function of gate charge; typical values

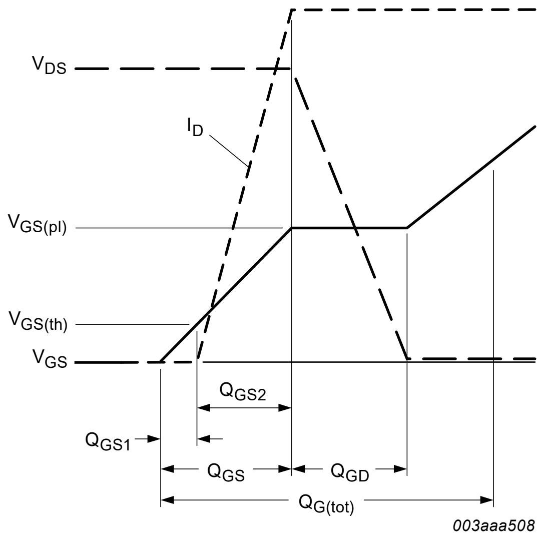
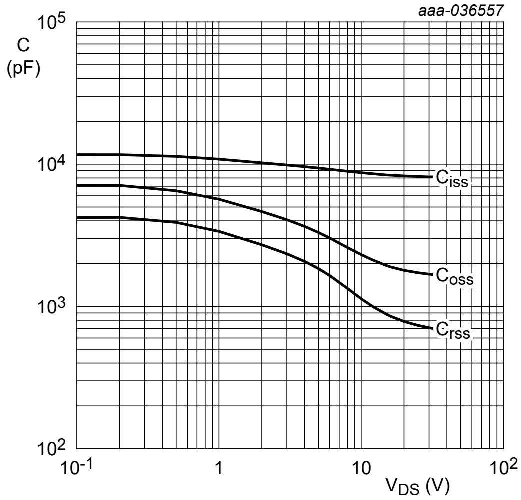


Fig. 16. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

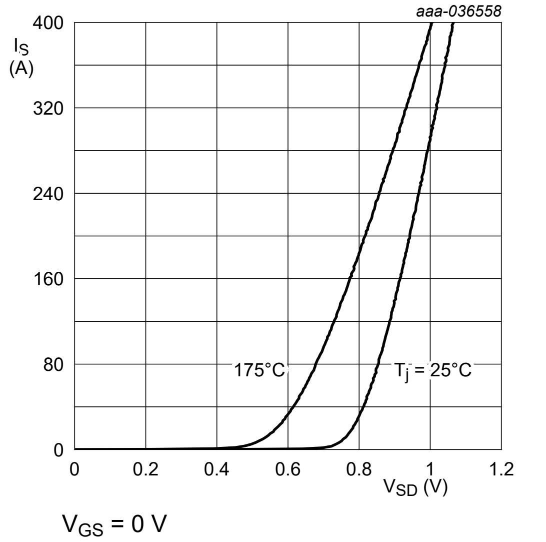


Fig. 18. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

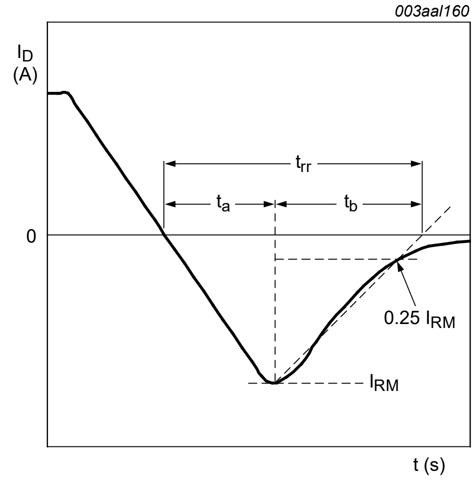
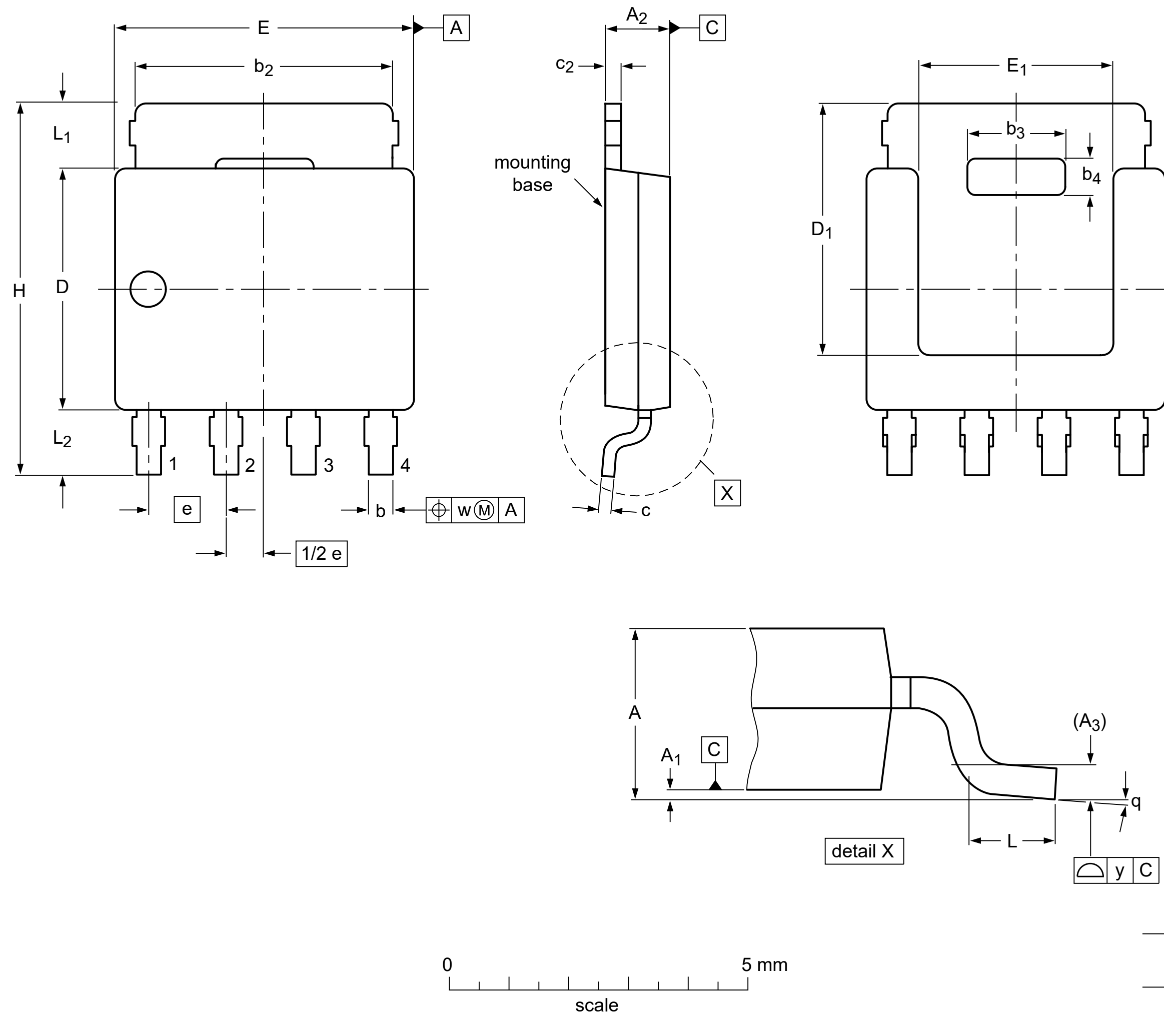


Fig. 19. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3			8°
	nom				0.25											1.27					0.25	0.1	
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 20. Package outline LFPAK56; Power-SO8 (SOT669)

12. Soldering

Footprint information for reflow soldering **SOT669**

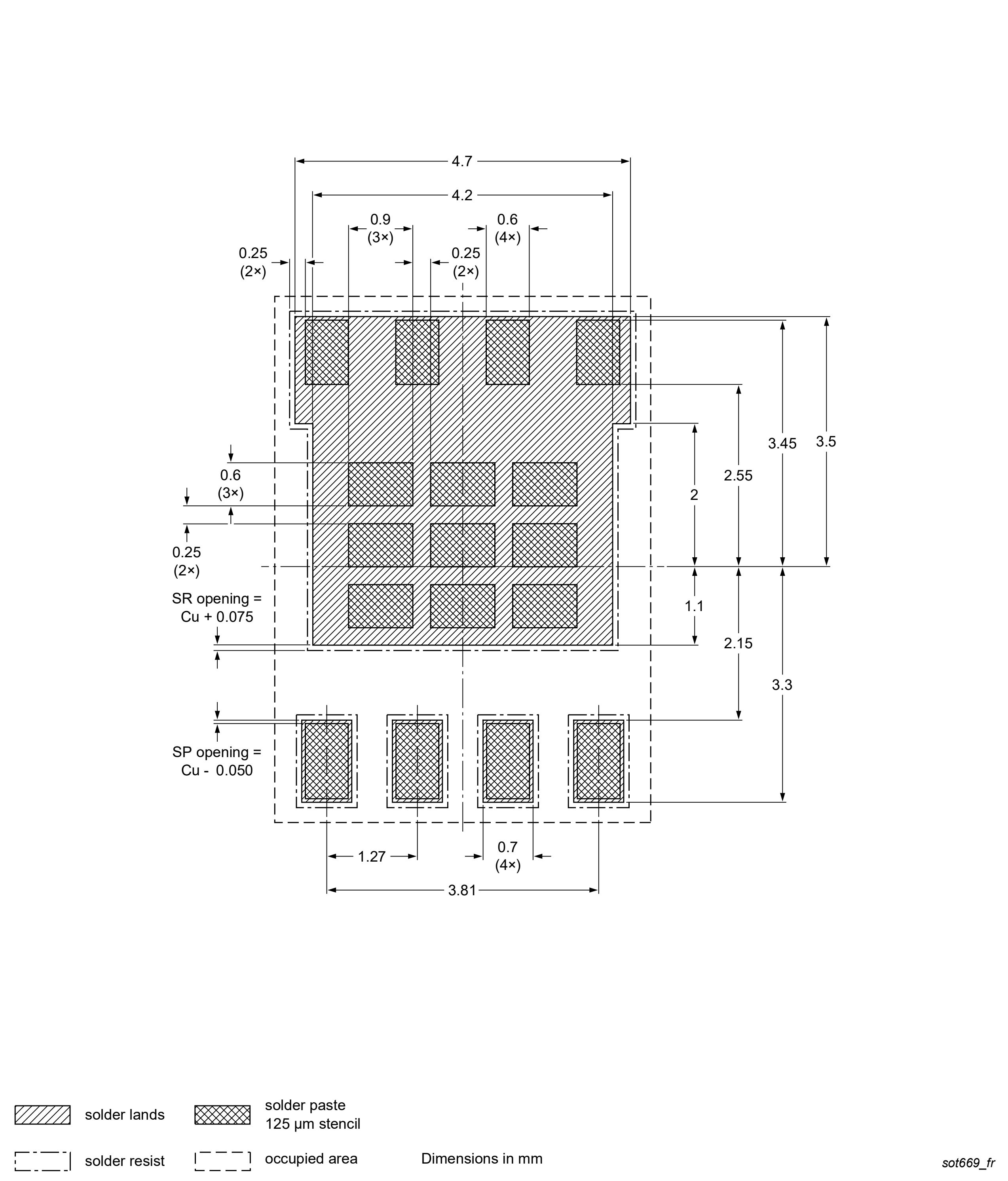


Fig. 21. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package **SOT669**

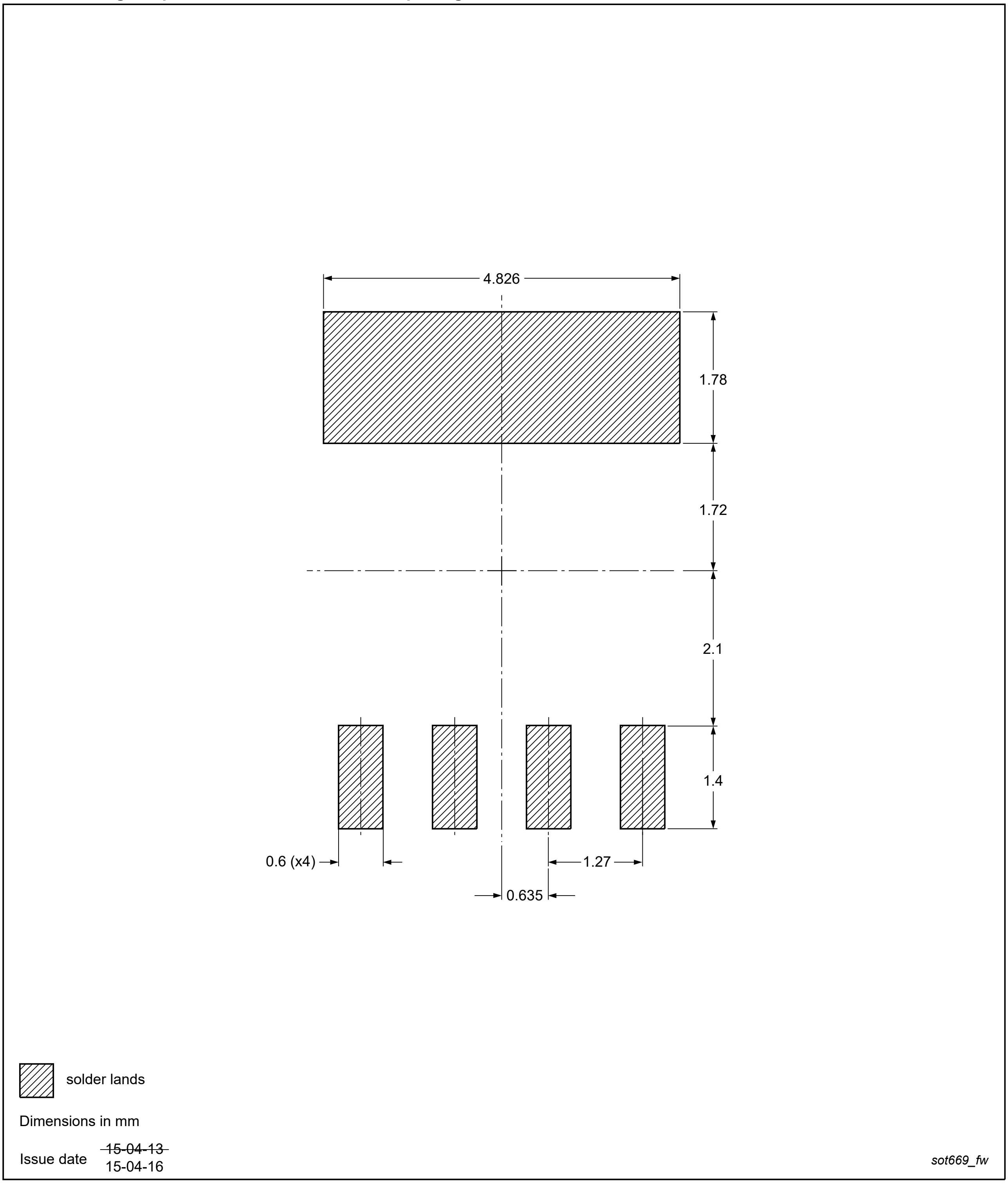


Fig. 22. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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